Με τη συγχρηματοδότηση της Ελλάδας και της Ευρωπαϊκής Ένωσης

Δράση ΕΡΕΥΝΩ – ΔΗΜΙΟΥΡΓΩ – ΚΑΙΝΟΤΟΜΩ

Συγχρηματοδότηση από την Ευρωπαϊκή Ένωση και τους εθνικούς πόρους μέσω του Ε.Π. Ανταγωνιστικότητα, Επιχειρηματικότητα & Καινοτομία (ΕΠΑνΕΚ)

RADAR

“ Ετερογενής Τρισδιάστατη Ολοκλήρωση με χρήση ρηξικέλευθων νανοτεχνολογιών για τη νέα γενιά μικροκυματικών πομποδεκτών ισχύος ”

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1. Αντικείμενο της Αναφοράς

Αντικείμενο της παρούσας αναφοράς είναι η καταγραφή των ενεργειών που έχουν γίνει κατά τη διάρκεια του πρώτου έτους του προγράμματος για τη διάχυση των αποτελεσμάτων της έρευνας στα πλαίσια της ΕΕ2 του ΡΑΝΤΑΡ. Είναι αναμενόμενο η ποσότητα των ενεργειών αυτών να είναι σχετικά περιορισμένη για τους πρώτους 12 μήνες.

Αρχικά δημιουργήθηκε το ΙΤΕ ιστότοπος που είναι συνεχώς ενημερωμένος. Ο ιστότοπος παρουσιάζει τα προφίλ των εταίρων της κοινοπραξίας και τις δράσεις διάχυσης. Η τακτική προώθηση των ειδήσεων και των εκδηλώσεων του έργου γίνεται μέσω αυτού που θα παραμείνει ενεργός για τουλάχιστον τέσσερα ακόμη χρόνια.

Η κοινοπραξία φροντίζει τα αποτελέσματα να δημοσιεύονται σε περιοδικά μεγάλου αντικτύπου και να ανακοινώνονται σε σημαντικά διεθνή συνέδρια.

Επίσης, στόχος της κοινοπραξίας είναι η διάδοση των επιτευγμάτων του έργου σε διεθνή τεχνικά φόρουμ και σε ημερίδες στα πλαίσια των δράσεων της εθνικής υποδομής Innovation-EL και της ελληνικής επιστημονικής εταιρείας Micro & Nano. Επιπλέον θα γίνουν προσπάθειες για διάχυση προς τις σχετικές βιομηχανικές και ακαδημαϊκές οργανώσεις Public-Private Partnership (PPP clusters) της ΕΕ και άλλους φορείς όπως η European Defense Agency (EDA).

Η κοινοπραξία προτίθεται να οργανώσει θεματική ημερίδα για να διαφημίσει τα τεχνικά και επιστημονικά επιτεύγματα του έργου.

Οι δραστηριότητες προβολής του έργου και διάχυσης των αποτελεσμάτων του έργου περιλαμβάνουν και συμμετοχή σε εκδηλώσεις "ανοικτής ημέρας", παρουσιάσεις και ομιλίες κατά τη διάρκεια της "Βραδιάς του Ευρωπαίου Ερευνητή" και της "Μάθε περισσότερα, γίνε καλύτερος" εκπαιδευτικές δράσεις αφιερωμένες στα σχολεία. Φυλλάδια και δελτία θα παρουσιάζουν εκλαϊκευμένα τα αποτελέσματα του έργου στο ευρύ κοινό.

2. Ιστότοπος "RADAR"

2.1. ΕΙΣΑΓΩΓΗ

Ο ιστότοπος "RADAR" σχεδιάστηκε για να παρέχει πληροφορίες σχετικά με το έργο και για το πώς θα επιτευχθούν οι στόχοι του. Ο ιστότοπος του έργου "RADAR" διατίθεται στο https://radar-project.iesl.forth.gr/ και είναι προσβάσιμο από κινητές συσκευές. Ο ιστότοπος σχεδιάστηκε για να αναθεωρεί και να αναπτύσσει συνεχώς τις δραστηριότητες διάδοσης στο πλαίσιο του έργου και να επιτρέπει συνεχή βελτίωση.

Ο δικτυακός τόπος περιλαμβάνει δύο διαφορετικούς τομείς, αφενός, έναν ιδιωτικό χώρο, ο οποίος χρησιμοποιείται κυρίως ως χώρος αποθήκευσης εγγράφων και ανταλλαγής διαβαθμισμένων πληροφοριών και, αφετέρου, δημόσιος χώρος. Ο δημόσιος χώρος του ιστότοπου θα προωθήσει το έργο "RADAR" μέσω σχετικών πληροφοριών, συμπεριλαμβανομένων των στόχων του έργου, του ιστορικού εταίρου και των μη ταξινομημένων αποτελεσμάτων του έργου.

Όλοι οι εταίροι θα συμμετάσχουν συλλογικά στην επικαιροποίηση διάδοσης της ιστοσελίδας παρέχοντας ενημερωμένες πληροφορίες

2.2. ΣΧΕΔΙΑΣΜΟΣ, ΣΥΝΤΗΡΗΣΗ ΚΑΙ ΕΝΗΜΕΡΩΣΗ

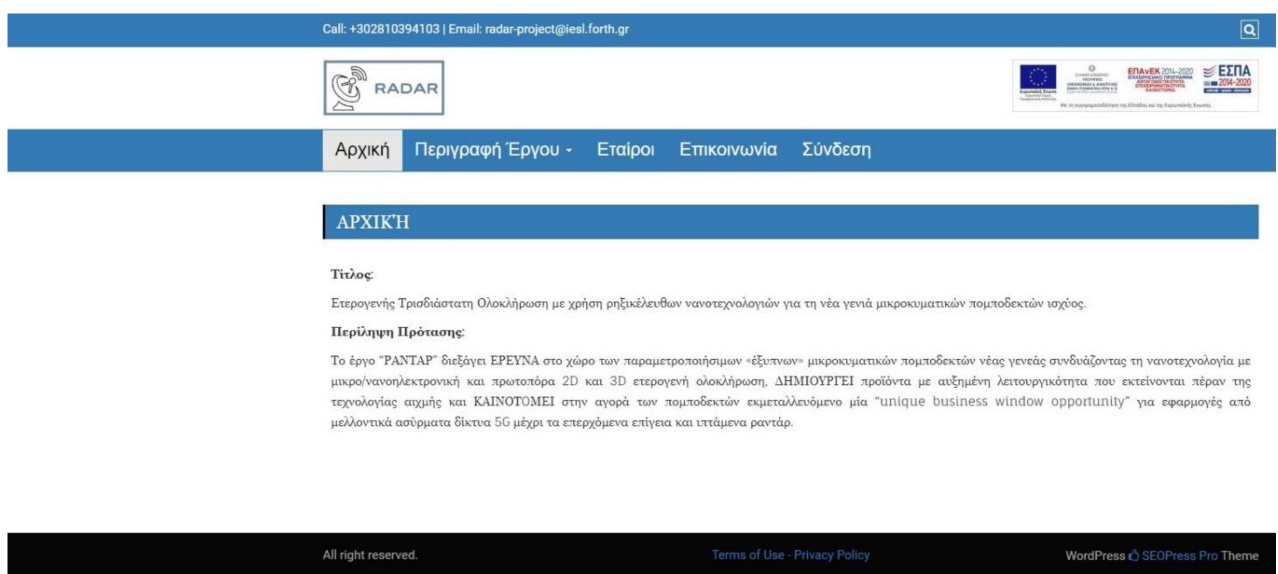
Ο ιστότοπος σχεδιάστηκε με έναν εύκολο τρόπο πλοήγησης, ο οποίος επιτρέπει στους χρήστες του ιστότοπου να μάθουν για το έργο και τα αποτελέσματά του, ειδήσεις κλπ. Όλα τα τμήματα του ιστότοπου έχουν στην κορυφή το λογότυπο RADAR (στα αριστερά) και μια αναφορά στη χρηματοδότηση εργαλεία (στα δεξιά).

Η ιστοσελίδα φιλοξενείται και διοικείται από την Ομάδα Μικροηλεκτρονικής Έρευνας (MRG) του Ινστιτούτου Ηλεκτρονικής Δομής και Λέιζερ (IESL) του Ιδρύματος Τεχνολογίας και Έρευνας (ΙΤΕ). Ένα αφοσιωμένο μέλος του προσωπικού της MRG επικαιροποιεί τακτικά τον ιστότοπο, μοιράζεται ειδήσεις, πληροφορίες σχετικά με εκδηλώσεις του έργου, παρουσιάσεις και άλλα σχετικά με το υλικό του έργου.

Ο ιστότοπος κατασκευάστηκε χρησιμοποιώντας το WordPress. Το WordPress είναι ένα ελεύθερο και ανοικτού κώδικα σύστημα διαχείρισης περιεχομένου (CMS) βασισμένο σε PHP και MySQL. Μεταξύ άλλων πλατφορμών, το Wordpress είναι μια δημοφιλής, καλά υποστηριζόμενη πλατφόρμα δημοσίευσης blogging και έχει μια μεγάλη κοινότητα που θα ελαχιστοποιήσει το ποσό της πολύπλοκης προσαρμογής που θα χρειαστεί να κάνει ο Συνεργάτης του Έργου.

2.3. ΔΙΑΡΘΡΩΣΗ ΙΣΤΟΣΕΛΙΔΑΣ

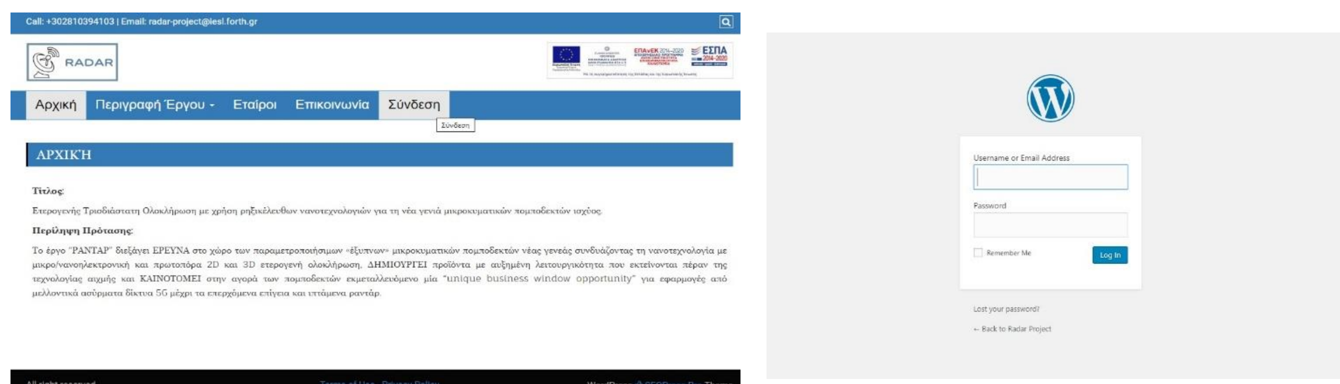
Ο δημόσιος χώρος έχει σχεδιαστεί για να εξασφαλίσει τη δημόσια προβολή των επιτευγμάτων και των αποτελεσμάτων του RADAR. Ο δημόσιος χώρος περιλαμβάνει πέντε κύριες σελίδες, όπως φαίνεται στο Σχήμα 1: Αρχική σελίδα, περιγραφή της εργασίας, συνεργάτες, διάδοση, επικοινωνία και μια καρτέλα "Σύνδεση" για να έχουν πρόσβαση οι συνεργάτες στην ιδιωτική περιοχή (προστατεύεται με κωδικό πρόσβασης). Αγγλικά είναι η γλώσσα που επιλέξατε.



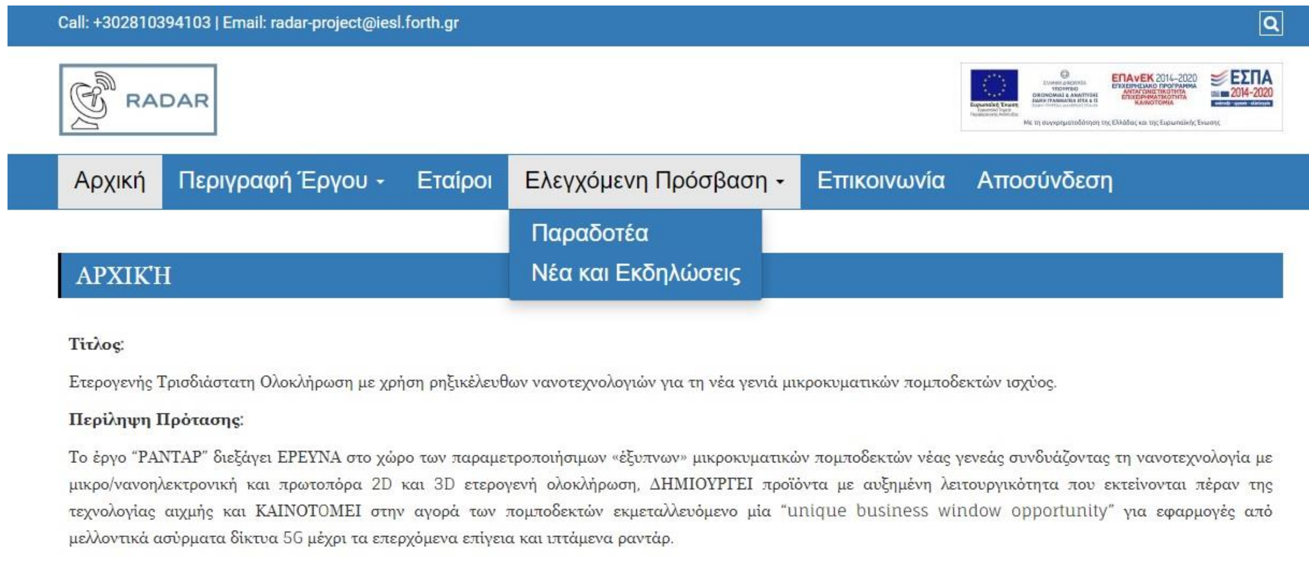
Σχήμα 1: Στιγμιότυπο οθόνης της αρχικής σελίδας του ιστότοπου "RADAR"

- Η σελίδα **«Αρχική»** παρέχει γενικές πληροφορίες για το έργο «RADAR».
- Η σελίδα **«Περιγραφή Έργου»** παρουσιάζει το αντικείμενο, τους στόχους και την μεθοδολογία υλοποίησης του έργου.
- Η σελίδα **«Εταίροι»** παρουσιάζει τις επωνυμίες των εταίρων που συμμετέχουν στο έργο, καθώς και τις συντομογραφίες μαζί με τις περιφέρειες του κάθε φορέα.
- Η σελίδα **«Επικοινωνία»** παρουσιάζει πληροφορίες (τηλέφωνα και διεύθυνση επικοινωνίας) που σχετίζονται με τον συντονιστή του προγράμματος.
- Η σελίδα **«Σύνδεση»** δίνει την δυνατότητα πρόσβασης στην ιδιωτική περιοχή του έργου «RADAR». Οι εταίροι ανακατευθύνονται στη σελίδα σύνδεσης και ζητούν τη σύνδεσή τους και τον κωδικό πρόσβασής τους για να μπουν στην περιοχή.

Ο ιδιωτικός χώρος έχει σχεδιαστεί ως μια ενιαία πλατφόρμα εργασίας μόνο για εξουσιοδοτημένους χρήστες μόνο. Ο χώρος αυτός χρησιμοποιείται για την κοινή χρήση όλων των εμπιστευτικών εγγράφων και η πρόσβαση σε αυτήν απαιτεί διαδικασία σύνδεσης όπου όλοι οι εταίροι έχουν λάβει ο καθένας ξεχωριστά από ένα αναγνωριστικό ονόματος και κωδικό πρόσβασης. Στα παρακάτω Σχήματα 2 και 3 είναι στιγμιότυπα οθόνης της ιστοσελίδας του Έργου «RADAR».



Σχήμα 2: Για να έχει κάποιος χρήστης/εταίρος πρόσβαση στην ελεγχόμενη περιοχή της ιστοσελίδας, θα πρέπει να κάνει σύνδεση με χρήση ονόματος και κωδικού που του έχει δοθεί από τον διαχειριστή της ιστοσελίδας.



Σχήμα 3: Ο χρήστης/εταίρος της ιστοσελίδας όταν συνδεθεί επιτυχώς στην ελεγχόμενη περιοχή έχει πρόσβαση στις κατηγορίες «Παραδοτέα» και «Νέα και Εκδηλώσεις»

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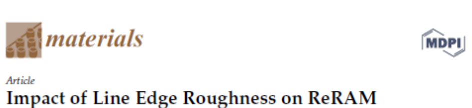
3. Δημοσιεύσεις σε διεθνή περιοδικά και συνέδρια (acknowledging RADAR)

3.1. Διεθνή Περιοδικά

1. Vassilios Constantoudis, George Papavieros, Panagiotis Karakolis, Ali Khiat, Themistoklis Prodromakis and Panagiotis Dimitrakis, "Impact of Line Edge Roughness on ReRAM Uniformity and Scaling", Materials 2019, 12, 3972; doi:10.3390/ma12233972



Article

Impact of Line Edge Roughness on ReRAM Uniformity and Scaling

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Abstract: We investigate the effects of Line Edge Roughness (LER) of electrode lines on the uniformity of Resistive Random Access Memory (ReRAM) device areas in cross-point architectures. To this end, a modeling approach is implemented based on the generation of 2D cross-point patterns with predefined and controlled LER and pattern parameters. The aim is to evaluate the significance of LER in the variability of device areas and their performances and to pinpoint the most critical parameters and conditions. It is found that conventional LER parameters may induce >10% area variability depending on pattern dimensions and cross edge/line correlations. Increased edge correlations in lines such as those that appeared in Double Patterning and Directed Self-assembly Lithography techniques lead to reduced area variability. Finally, a theoretical formula is derived to explain the numerical dependencies of the modeling method.

Keywords: Resistive Random Access Memory (ReRAM); Line Edge Roughness (LER); variability; uniformity; modeling; lithography

1. Introduction

Resistive Random Access Memory (ReRAM) technologies are considered as one of the most promising candidates for future nonvolatile memory (NVM) applications due to their high memory capacity [1], their simple two terminal architecture, and their excellent scalability [2]. ReRAM cells can be programmed faster than current NVMs and at lower voltages, overall leading to a significant reduction in energy consumption per bit [3]. The cross-point metal-insulator-metal (MIM) cell simple structure requires very low thermal budget and thus can be integrated easily in the current CMOS Back End of Line (BEOL) processing steps [4]. Large memory blocks have been implemented and demonstrated, following the cross-point architecture [5]. The cross-point area F × F, F is the lithography node, can be as small as 2 nm × 2 nm [6] leading to a very small cell footprint (area/bit) $4F^2$. Conductive AFM experiments have demonstrated that the ReRAM memory cell area can be as small as that of an AFM tip [7]. In addition, the 3D stacking of different memory layers [8] reduces the cell's footprint to $4F^2/n$, where n is the number of the stacked memory layers, and hence severely increases the density of the ReRAM memory chips. Moreover, the ReRAM cell can be used to realize memristive devices to implement new computing paradigms like neuromorphic [3,9], reconfigurable electronics [10], and logic-in-memory [11].

The uniformity of the cell SET and RESET voltages (V_{SET} and V_{RESET}, respectively) is a key-challenge to large-scale manufacturing of ReRAM technology. Up to now, it has been mainly related to the stochastic nature of conducting a filament creation process. Remedies that have been proposed consider (a) engineering of electrode/oxide interface [12], (b) inserting seeds (nanoparticles) in the oxide bulk [13], and (c) reduction of the size of cell area [14]. The latter is related to the scaling trends of ReRAM devices and is a great advantage of this technology since scaling down the dimensions of a ReRAM cell goes with the increase in performance uniformity due to the mitigation of stochastic filament formation. Thus, scalability is generally considered an advantage of ReRAM owing to the filamentary conduction and switching mechanisms. The effect of the reduction of the cell size area to the various parameters of ReRAM operation is an active matter of debate. To that end, in Reference [14] a simplified analytical model to describe the area and thickness scaling of forming voltage is proposed. Binary-oxide ReRAM scalability performance has drawn the attention of various groups. The general scaling trend of the high and low resistance states from various metal oxide ReRAMs has been presented in Reference [15]. The dependence of the scaling area on various ReRAM operation parameters (Resistance, SET/RESET current, SET/RESET voltage) has been studied thoroughly for HfO_x [16,17], TaO_x [18], SiO_2 [19], ZrO_2 [20], and recently for Al_2O_3 [21] and for TiO_2 [22]. Similar scalability issues have been examined for perovskite material-based ReRAMs, such as $SrTiO_3$ [23], and metal nitrides, such as AlN [24] and NiN [25].

However, up to now no special attention has been paid on deviations frompattern's uniformity induced by the fabrication process and material properties. In CMOS technology, one of the most important sources of such deviations from manufacturing uniformity is related to the Line Edge Roughness (LER). LER is actually the sidewall roughness of pattern lines manufactured via standard lithographic rules, as often observed via top-down SEM images. The effect of LER becomes more evident as the size of devices is reduced, which is the reason for the recent upsurge of interest in LER control in modern <20 nm semiconductor manufacturing [26]. Obviously, LER is responsible for the area variability of devices in a crossbar (Xbar) array and, furthermore, the cell-to-cell and wafer-to-wafer variability that appear in the operation parameters of ReRAM memory cells in Xbar arrays. More specifically, as mentioned in [15], the resistance at HRS increases as the inverse of the area cell A (i.e., R_{HRS}~1/A) while the reset current increases as A decreases. Furthermore, the reduction of the cell size A attributes to local heating causing faster switching times [17]. In addition, forming and SET voltages also increase as the cell area A decreases [17]. These detrimental LER effects are expected to become stronger increasing the size of the memory crossbar array: The larger the memory array the stronger the effects are.

The importance of LER is justified by the evaluation of its effects on device performance. This can be done through carefully designed experiments or modeling/simulation studies. Results from such studies help defining the specifications for allowed LER in roadmaps and factory production lines. Clearly, the level of acceptable LER is defined by the operating constraints of distinct applications that employ nanoscale devices. Up to now, several modeling and experimental investigations have been performed for conventional MOSFET [27–30] and FinFET [31,32] devices. On the contrary, very few studies have been devoted to the LER effects on memory and especially ReRAM devices. In the fabrication of ReRAM and especially in the cross-point configurations, the LER of metallic lines may affect device performance through the induced variability to the cross-point cell areas and consequently to the device resistance.

Furthermore, it was recently realized that LER characteristics are sensitive to the applied lithographic technique [33]. The main point of differentiation comes from the degree of correlations between the fabricated edges and lines. In EUV patterns, for example, the nearby lines and edges are totally uncorrelated while in Multiple Pattern (MP) techniques correlations are induced mainly between the edges of each line, whereas lines are still independent at least for Double Patterning (DP) schemes. On the contrary, in Directed Self-Assembly (DSA) lithography even nearby lines exhibit correlated fluctuations arising from the very self-assembly nature of the process and the sidewall

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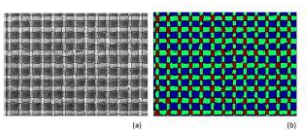
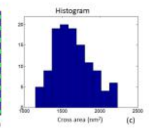
roughness of grapho-epitaxy grating used for the alignment of lines. Therefore, LER modeling should always consider such aspects and adjust the modeled patterns according to the considered lithography. Up to now, the modeling strategies for the generation of line edges similar to the fabricated ones are based on inverse Fourier techniques, where no correlations are taken into account between edges or lines [34,35].

In order to get a better picture of the LER impact on cell area uniformity, one can observe Figure 1a where several ReRAM prototypes, of cross-point architecture, were fabricated by e-beam lithography and are depicted in a top-down SEM image. Furthermore, on the same SEM image the detected edges defining the borders of electrode lines are illustrated with black color. It can be clearly seen that the roughness of the metal edges induces non-uniform cell areas (see Figure 1b). The distribution of the cell areas is presented in Figure 1c where one can notice the wide distribution of cell area values. This data supports our claim that LER needs to be considered carefully for achieving a uniform and reliable ReRAM technology and deserves more investigation.





Histogram
Cross area (nm²)
(a) (b) (c)

Figure 1. (**a**) A top-down SEM image of a cross-point pattern with the detected edges of the vertical and horizontal metal lines defining the crossing areas, (**b**) a colored illustration of the SEM image to show the crossing areas more clearly in red color and the metal lines in green color, (**c**) the histogram of the calculated cross-point area values in nm^2. The Line Edge Roughness (LER) (average root mean square (rms) value) of the vertical and horizontal lines was measured and found equal to 2.6 and 3.8 nm, respectively. The width of the distribution of cross areas (standard deviation) is found to be almost 16% of the mean value. Therefore, the commonly used three times this value reaches almost 50% of the mean value indicating the strong impact of LER of metal lines to the nonuniformity of Resistive Random Access Memory (ReRAM) device areas.

In this paper, we evaluate the effects of LER of metallic lines on the device area uniformity, which is critical for the device performance. Three types of line patterns are considered corresponding to EUV, Multiple Patterning (MP), and DSA patterns to compare these with respect to their vulnerability to LER defect. In Section 2, the modeling methodology is presented and explained. The results of the modeling approach to EUV, MP, and DSA-based patterns are shown and discussed in Section 3. In the end of the same section, we also derive an analytical formula capturing the numerical modeling results with quantitative success. The last section, Section 4, summarizes the findings of the paper and draws the main conclusions.

2. Modeling Methodology

2.1. Background of Modeling: LER Characterization in Different Lithography Techniques

LER is usually defined as the deviation from smoothness (flatness) of the sidewalls of resist or substrate lines. In top-down SEM images, this deviation is reflected through the roughness of the edge defining the 2D borders of the line region. In the initial stages of LER studies, line edge points were considered uncorrelated and the main emphasis was given on the measurement of their root mean square (rms) value (standard deviation), quantifying the wideness of the edge point distribution. However, quite early, the characterization scheme was enriched with more parameters and functions

aiming to capture and quantify the spatial/lateral or frequency aspects of LER preserving the dominant significance of rms. To this end, a three-parameter model has been proposed [26] consisting of rms value, correlation length ξ, and roughness exponent α (related to the fractal dimension $d = 2-\alpha$) and extensively used in different applications. The first parameter rms quantifies the vertical aspects of LER and is calculated by the standard deviation of the edge points about their mean value. The other two parameters (ξ and α) focus on the spatial aspects of LER. The correlation length ξ quantifies the window inside which the edge points can be considered correlated, i.e., they have similar deviations from the mean value, and delivers a statistical estimation of the mean width of edge fluctuations. Large values of ξ mean slowly varying edges while small values characterize more jagged edges. The correlation length is normally calculated through the autocorrelation function R(r) as the distance r at which R(r) is lowering beneath 1/e, i.e., $R(\xi) = 1/e$ [36]. The roughness exponent $0 < \alpha < 1$ quantifies the contribution of various scales and frequencies to the whole LER. When α takes on low values, high frequencies dominate, whereas when it approaches 1, the edge becomes smoother at small scales and the importance of high frequency fluctuations is being lessened.

When a more detailed function-like characterization of spatial and frequency LER aspects is demanded, the Power Spectrum (PS) and the Height–Height Correlation Function (HHCF) can be calculated and elaborated. The overall shape of these functions is linked to the three-parameter model, when LER obeys a self-affine fractal symmetry [36]. The effects of LER on line width fluctuations (usually called Line Width Roughness (LWR)) complete the overall picture of the conventional approach to LER metrology. The relationship between LER and LWR metrics has been clarified and it can be shown that the low frequency LWR could have a significant contribution to the total budget of local Critical Dimension Uniformity (CDU). This effect has underlined the importance of estimating the PS of LWR, which quantifies the contribution to LWR from different frequency areas. A detailed presentation of the conventional LER and LWR metrology can be found in [26].

Nevertheless, during the recent years significant changes in lithographic landscape have been evidenced. The conventional scaling down of feature dimensions, based on the optimization of wavelength and Numerical Aperture (NA), has been replaced by a more etch-based and material-driven resolution enhancement, which duplicates the density of patterns through successive deposition and etching steps. The family of these MP techniques is currently used in high volume manufacturing in semiconductor industries. Additionally, the concept of self-assembly of block copolymers has been employed in lithography research in the last 10 years due to its ability to easily provide line/space patterns with widths less than 20 nm. The DSA lithography has seen an upsurge and very important advances have been performed in defect reduction and scaling improvement. However, what is usually missing is the effect that these new lithographic approaches have on LER and its metrology characterization. The key aspect of these effects is the lateral (across line direction) correlations they introduce in line/space patterns. In the EUV lithography patterns, the LER of edges are uncorrelated and no propagation of edge fluctuations is noticed between the edges of a line or the nearby lines of a pattern. On the contrary, in MP lithography patterns, the edges of the same line fluctuate in a correlated manner forming wiggling lines. A more dramatic change is observed in DSA patterns. Here, not only the line edges but also the lines themselves present correlations in the way they fluctuate. To capture these new aspects of LER, an extended framework for LER/LWR metrology has been proposed and elaborated based on the c-factor parameter, function, and correlation length. A detailed presentation and examples of application of these metrics can be found in [35].

2.2. Implementation of Modeling

The key idea of our approach is to model LER effects in cross-point area statistics using the 2D projections of the real 3D patterns, as they are shown in top-down SEM images similar to that in Figure 1. The assumption behind this approach is that 3D morphological variations do not have an important contribution to LER impact on device variability. This assumption is supported by

recent observations according to which the sidewall roughness of lithographic lines does not change significantly along *z*-direction since it exhibits a curtain-like morphology [37].

The modeling methodology is implemented in three steps. First, the structural parameters of the cross-point pattern are defined including line width (Critical Dimension, *CD*) and pitch values. The numbers of both vertical and horizontal lines are included in the modeling as well as. These parameters can differ in vertical (y) and horizontal (x) line patterns, though throughout this study we mainly consider the symmetrical case where $CD_X = CD_Y$ and $pitch_x = pitch_y$. Based on these parameters, the ideal smooth pattern can be generated as shown in Figure 2a. In the second step, the smooth edges are converted to rough edges characterized by the input predetermined roughness parameters: rms, ξ, α. The generation of rough edges is made using the convolution method and requires the use of a model function for the Power Spectrum or the Height–Height Correlation Function. Here, we extensively use the following HHCF $G(r)$ that is also used in self-affine rough processes [34,38]:

$$G^2(r) = 2rms^2(1 - e^{(-\frac{r}{\xi})^{2\alpha}}). \quad (1)$$

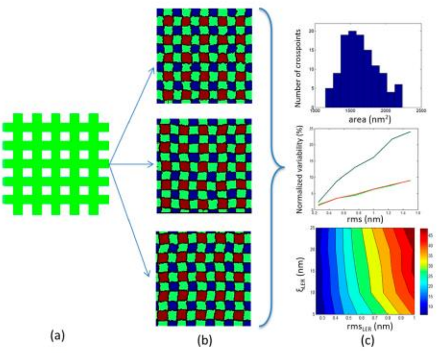


Figure 2. A schematic view of our modeling steps for LER effects on device uniformity. First, a pattern is formed (**a**) with the given parameters (Critical Dimension (*CD*), pitch, number of lines), then (**b**) roughness is imposed on the edges to get LER with predefined parameters, and then in (**c**) the statistical analysis of cross areas A_i is performed to get the normalized standard deviation $\sigma(A)$ versus LER parameters.

The successive application of the convolution method with no further processing of edges produces uncorrelated edges, which then can be positioned according to *CD* and pitch values to build the whole cross-point pattern. The generated pattern can be used to model the 2D projection of line/space

structures fabricated by mask-based lithographic rules (EUV or 193i). When MP or DSA patterns are sought, we may add correlation either between the edges of the same line or to expand these between nearby lines to get DSA-like patterns. Figure 2b shows examples of such patterns with controlled LER parameters as well as cross-edge and cross-line correlations.

In the third step of our methodology, we measure the areas of cross-points A_i, $I = 1, \ldots, N_x N_y$ where horizontal and vertical lines overlap in the considered rough pattern of $N_x x N_y$ lines. Then we calculate the normalized standard deviation $\sigma(A)$ of the A_i values ($= std(A_i)/<A_i>$) and we plot it for various dimensional and LER parameters and edge/line correlation levels (see Figure 2c).

3. Results and Discussion

The results of our modeling calculations are collectively illustrated in Figure 3, which displays six contour plots. Each one of these plots depicts the dependence of $\sigma(A)$ on the LER parameters rms and ξ, given that these parameters are considered to quantify LER according to the last editions of ITRS [39]. In all runs, the roughness exponent α is kept fixed to 0.5 in conformity with more experimental measurements. We consider that both horizontal and vertical lines have similar LER parameters. The left column of Figure 3a,c,e contains the contour plots with *CD* = 20 nm and pitch = 40 nm while the right column shows the results when the pattern scales down at *CD* = 10 nm and pitch = 20 nm. The different rows account for increased levels of horizontal (cross-line) correlations between edges and lines. In the first row, both edges and lines are generated to be uncorrelated to capture the case of mask lithography line structures (EUV and 193i). The second row contains the results for cross-point patterns where the edges of each line are correlated, though the lines themselves fluctuate independently. The latter pattern resembles the line/space structures acquired by Double Patterning Lithography techniques. In the third row, the contour plots concern model patterns where the horizontal correlations propagate across both edges and lines similarly to what is happening in DSAL.

From the contour plots of Figure 3, we are able to extract conclusions and discuss the following issues: (a) the dependence of $\sigma(A)$ on LER parameters rms and ξ, which seems to exhibit a similar pattern in all cases, (b) the effects of scaling down the pattern dimensions, and (c) the effects of cross-edge and line correlations.

3.1. The Impact of LER Parameters Rms, ξ

The overall shape of all contour plots in Figure 3 is characterized by the dominance of vertical contour lines, which reveal the stronger dependence of area uniformity on rms with respect to that of the correlation length. In order to focus on the dependencies themselves, we take a horizontal and vertical cross-section of the contour diagrams and the outcome plots are shown in Figure 4 for all considered cases. One can easily notice the linear increase of $\sigma(A)$ with rms value in all cases, while the effects of ξ are sublinear justifying the dominant role of rms in the effects of LER on cross area uniformity. In other words, both rms and ξ in LER degrade device area variability with rms exhibiting the primary effect.

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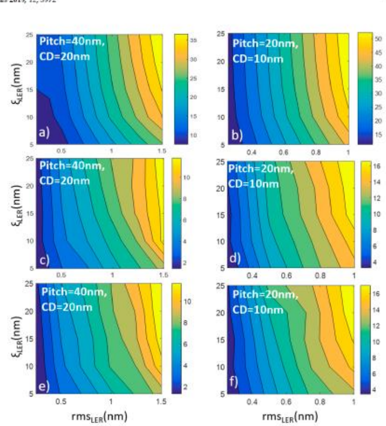

Figure 3. Contour plots of $\sigma(A)$ vs. rms_{LER} and correlation length ξ_{LER}. Left (**a**,**c**,**e**) and right (**b**,**d**,**f**) columns contain the plots for CD = 20 nm and CD = 10 nm, respectively. Furthermore, in the second (**c**,**d**) and third (**e**,**f**) row the calculations have been done considering patterns with correlated edges and correlated edges and lines respectively.

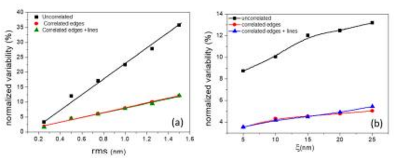

Figure 4. An example of the dependence of the normalized variability $\sigma(A)$ on (**a**) rms and (**b**) ξ for typical parameters. One can notice the linear and sublinear increase of $\sigma(A)$ vs. rms and ξ, respectively.

3.2. The Impact of Scaling Device Size

The comparison of the contour plots of the left and right columns reveals that the scaling down of pattern dimensions by a factor 2 (quadrupling of device density) is associated with an almost doubling of normalized area variability $\sigma(A)$. This observation holds at all rows, i.e., it is independent of the level of edge/line correlations.

3.3. The Impact of Edge and Line Correlations

When MP or DSA lithographic techniques are used for ReRAM pattern fabrication, edges and lines exhibit cross-correlations, i.e., they fluctuate in a correlated manner. The second and third rows of Figure 3 show the contour plots for $\sigma(A)$ when the pattern exhibits only edge and both edge and line correlations, respectively. Although the pattern of contour lines remain almost unaltered, the $\sigma(A)$ values demonstrate a clear reduction with respect to the values of first rows approximately by a factor 3. The amount of reduction is similar at the contour plots of the second and third rows, which indicates that the critical correlations for variability drop are those between edges. The cross-line correlations do not seem to play any role in LER-induced degradation effects on area uniformity.

3.4. Analytical Formula for LER Effects on Area Variability

The dependencies of $\sigma(A)$ on LER parameters found by modeling and shown in Figure 3 can be captured in an analytical formula which can be derived as follows: For patterns with smooth edges (no LER) the cross-point areas are fixed in all devices and equal to $A_i = CD_X CD_Y$ with no variability at all. When we consider rough edges, LER induces local variability in line widths, which is usually called Line Width Roughness (LWR). Therefore, each crossing area can be roughly characterized by $A_i = CD_{ix}CD_{iy}$, where CD_{ix} and CD_{iy} are the average line widths across x- and y-directions enclosed in the i-th crossing area. Due to LER and LWR, CD_{ix} and CD_{iy} change randomly from area to area. If we assume that on average this variability is similar to both vertical and horizontal lines, we get for the $\sigma(A)$:

$$\sigma(A) = \frac{std(A_i)}{\langle A_i \rangle} \approx \frac{\sqrt{2} std(CD_i)}{\langle CD_i \rangle}. \quad (2)$$

The relationship of CD variance ($std^2(CD_i)$) with local and total variances of LWR values has been studied extensively in LER literature and the following formula can be proven [20]:

$$std^2(CD_i) + \langle rms^2_{LWR}(CD_i) \rangle = rms^2_{LWR}(total), \quad (3)$$

where $rms_{LWR}(total)$ is the rms value of LWR for the total lines included in model patterns, which assume to get sufficiently large lengths so that the rms_{LWR} value stabilizes at a fixed value, and $\langle rms^2_{LWR}(CD_i) \rangle$ is the mean variance of LWR calculated inside the segments of length CD_i and averaged over all considered segments.

In order to get the relationship of $\sigma(A)$ with the input LER parameters, we need to pass from LWR to LER parameters. This can be achieved through the following formula connecting LWR and LER assuming similarity between left and right LER:

$$rms^2_{LWR} = 2(1-c)\, rms^2_{LER}. \quad (4)$$

Here, c is the c-factor quantifying the cross-correlations between the left and right edges of lines. For totally uncorrelated edges, $c = 0$, whereas for fully correlated (anti-correlated), $c = 1$ (−1) [26,33]. By combining (2), (3), and (4) we read:

$$\sigma(A) = \frac{2}{\langle CD_i \rangle} \sqrt{(1-c)(rms^2_{LER}(total) - \langle rms^2_{LER}(CD_i) \rangle)}. \quad (5)$$

The Formula (5) can be further processed in the case of edges with exponential autocorrelation functions (roughness exponent $\alpha = 0.5$) since for such edges it holds that

$$rms^2_{LER}(CD) = rms^2_{LER}(total)[1 - \frac{2\xi}{CD}(1 + \frac{\xi}{CD}e^{-\frac{CD}{\xi}} - 1)]. \quad (6)$$

Inserting (6) into (5) we get the final formula for the dependence of $\sigma(A)$ on LER parameters:

$$\sigma(A) = 2\sqrt{2(1-c)}\, \frac{rms_{LER}}{CD} \frac{\xi}{CD} \sqrt{\frac{CD}{\xi} + e^{-CD/\xi} - 1}. \quad (7)$$

Equation (7) incorporates all the dependencies of normalized area variability on the dimensional parameters (CD), the principal LER parameters (rms_{LER}, ξ) and the level of edge correlations (c-factor). As expected from the numerical results, pitch and line correlations are not included since they have no impact. One can easily notice that the analytical Formula (7) predicts (a) the linear proportionality of $\sigma(A)$ to rms_{LER}, (b) the sublinear increase of $\sigma(A)$ with ξ, (c) the almost linear inverse proportionality impact of CD, and (d) the reduced effects of increased edge correlations on $\sigma(A)$ quantified by c through the factor (1-c).

In order to get a more quantified and complete comparison of the analytical prediction with the numerical results, we show in Figure 5a a contour plot with the dependencies of $\sigma(A)$ on LER parameters (rms, ξ) as derived by the analytical Formula (7). We have chosen $c = 0$ (no edge correlations) and CD = 20 nm, which are the parameters of the numerical contour plot of Figure 3a. One can clearly indicate the striking qualitative and quantitative similarity of two contour plots, which is more directly and quantitatively illustrated in Figure 5b where the difference of the numerical and analytical normalized variability $\sigma(A)$ is shown versus rms and ξ parameters. The difference is always very close to zero and justifies the predictive power of the analytical formula. The sole exception is for the small rms values lower than 0.5 nm where the analytical formula seems to underestimate the numerical results. However, the observed discrepancy is due to issues with the numerical results. More specifically, in order to simulate the real procedure where the LER effects are evaluated through the analysis of SEM images (see Figure 1), in the numerical modeling we pixelize the edge data by rounding the generated edge points from the generator algorithms. We have shown that this discretization (pixelization) process induces a noise impact on LER and causes an increase of the measured rms value as explained in [40]. Therefore, in these regimes with extremely small rms values, one should trust the predictions of the analytical Formula (7) more than the numerical results of the 2D modeling.

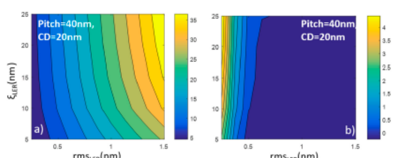

Figure 5. (**a**) Contour plot of the normalized variability $\sigma(A)$ cross-point areas versus the LER parameters rms and ξ for CD = 20 nm and c = 0 (no edge correlations) and (**b**) the difference of numerical and analytical predictions for $\sigma(A)$ for the standard parameters CD = 20 nm and c = 0. One can notice the striking similarity of numerical and analytical results with the slight exception of very small rms values where numerical results are biased due to pixelization of edge data.

The similarity between numerical results and analytical predictions was confirmed independently of CD and edge correlations. This means that the Formula (7) comprises a strong analytical tool to get control and deeper understanding of the LER effects on ReRAM area variability and performance degradation since it captures successfully the impact of LER main parameters (rms, ξ) as well as of the line width (CD) and edge correlations which may come from different lithography steps used in pattern formation.

4. Conclusions

In this work, we model the effect of lithographic performance parameters on the operation of ReRAM devices, assuming the main three lithographic techniques: EUV, MP and DSA. According to our numerical model, it is found that both rms and ξ in LER degrade device area variability with rms exhibiting the primary effect. Additionally, it is found that edge correlations favor area uniformity while the normalized area variability is doubled when the size becomes half of the initial. For comparison, an analytical model was developed also to simulate the impact of lithography performance parameters. The comparison between the 2D numerical and the analytical one reveals that both provide the same results independently of CD and edge correlations. Nevertheless, the analytical model is more accurate at extremely small rms values. In this context, the developed numerical and analytical models are highly valuable predictive tools for the integration of ReRAM devices at very small technology nodes.

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3.2. Διεθνή Συνέδρια

1. Evangelia Karagianni, Christina Lessi, “GaN wideband receiver for new generation applications”, Proceedings of the IIER International Coference, Bali, Indonesia, 30th -31st August, 2019.

GaN wideband receiver for new generation applications

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Abstract— Socially critical applications such as wireless and satellite communications, terrestrial and flying radars, cable TV and intelligent transport infrastructure have a significant impact on our everyday lives. The culmination of all modern technological applications is nowadays the Internet of Things (IoT). The LNA design that is presented is intended to be part of a transceiver, which will be placed in a hardware, offering better efficiency to new generation applications.

Index Terms—Gallium Nitride technology, Internet of Things, Software Defined Network, Low Noise Amplifier.

I. INTRODUCTION

Upcoming applications such as 5G, IoT, autonomous vehicles have upgraded requirements such as higher power, enhanced functionality and lower cost. Consequently, the transceivers need redesign, including innovative solutions, since GaAs is no longer capable of meeting the new requirements [1].

GaN technology seems to be a good choice to replace GaAs. Even though it is a relatively new technology, it has become very popular for high frequencies or high power devices.

Comparing GaN technology with the older ones, such as Si and GaAs, the results are presented in table 1 [2]:

1) The power density of a GaN material is almost 10 times higher than a Si material and it has good thermal conductivity.
2) GaN has 10 times higher breakdown field than Si or GaAs materials, so, devices can be smaller with high impedances.
3) It has lower dielectric constant than other materials, resulting in a lower intrinsic junction capacitance. When parasitics such as output capacitance and layout inductance are reduced, switching losses are reduced too, resulting in a higher frequency operation with the same loss [3] [4].
4) GaN HEMT has the highest saturated electron velocity of about 2.7x10⁷ cm/s among other semiconductor transistors [2] [5].
5) GaN transistors have increased efficiency, smaller size and fast switching. The smaller die size enables performance improvements in switching power applications.

Table 1. Comparison of GaN with other semiconductor materials

II. WIDEBAND APPLICATIONS AND SUGGESTED ARCHITECTURE

The technological revolution of the modern era enables the wireless communication system functions, from the antenna to the interface, to be executed and programmed by a single high level software language using a one hardware topology. These systems are the Software Defined Networks (SDN). An SDN has the ability to implement many different interfaces. However, since each standard can exploit a different frequency band, it is important the SDN to cover a large bandwidth.

Fig. 1: Multiple channel design

In order to achieve the wideband operation of the transceiver, its architecture will be based in multiple channels topology (figure 1). In this case, each channel operates in a wide range of frequencies, but still different from the range of the other channels. The signal entering the antenna is driven by a digital switch on the appropriate channel. By using this architecture, it is easily achievable to increase the system capacity by adding more receiving and transmitting channels of different RF carriers [6].

The paper is a part of the RADAR project "Heterogeneous 3D integration employ disruptive nanotechnologies for the next generation of smart power RF T/R modules", Project n° T1EΔK-00329, with co-financing of Greece and European Union

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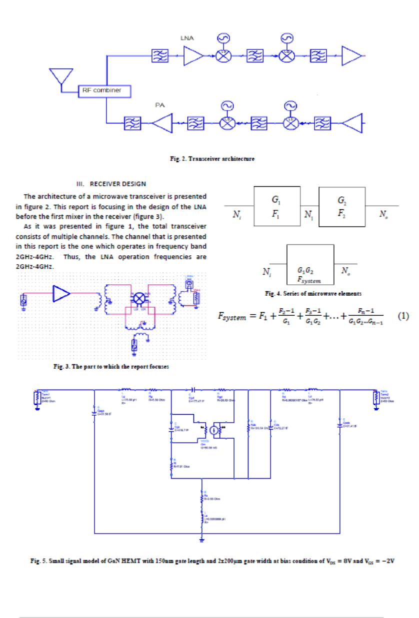

Fig 2. Transceiver architecture

III. RECEIVER DESIGN

The architecture of a microwave transceiver is presented in figure 2. This report is focusing in the design of the LNA before the first mixer in the receiver (figure 3).

As it was presented in figure 1, the total transceiver consists of multiple channels. The channel that is presented in this report is the one which operates in frequency band 2GHz-4GHz. Thus, the LNA operation frequencies are 2GHz-4GHz.

Fig 4. Series of microwave elements

$$F_{system} = F_1 + \frac{F_2-1}{G_1} + \frac{F_3-1}{G_1G_2} + \dots + \frac{F_n-1}{G_1G_2 \dots G_{n-1}} \quad (1)$$

Fig 3. The part to which the report focuses

Fig. 5. Small signal model of GaN HEMT with 150um gate length and 2x200um gate width at bias condition of V_{ds} = 0V and V_{gs} = −2V

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The most important characteristic of an LNA is the low level of noise that adds in the signal. If the receiver is depicted as a set of boxes in a raw (figure 4), each box represents an element of this receiver that has a gain and a noise level, then the total noise level is calculated by the equation 1. The equation explains that the noise of the first element is the most crucial for the total system noise, while the next elements noise is not that important since it is divided by the gain of all previous elements.

The receiver will be designed by using GaN technology. On figure 5 the small signal model of the GaN HEMT that will be used is presented [7]. Additionally, the S-parameters of the transistor are presented in figure 6.

The cascade topology will be used for the LNA design. The desesion of that topology is based on the benefits that it offers acording the output gain considering at the same time the low noise level [8]. The operasion prisciples are these which was described in equation 1. Furthermore, the matching circuit will have two diferent parts: the first one is the 2GHz matching circuit and the second one is the 4GHz matching circuit. This topology operates as it presented in figure 7. The two matching circuits leads to the proper operation of the LNA in the frequences between the edges. In figure 8 the complete LNA design is presented, while in figure 9 the noise figure and the S-parameters are presented.

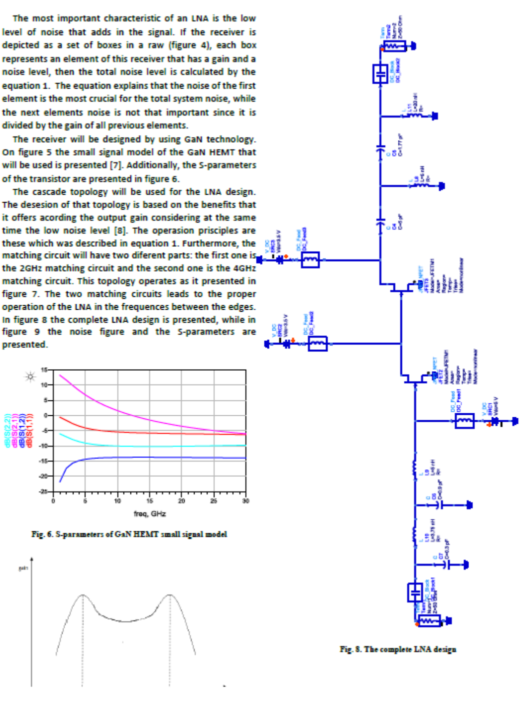

Fig. 6. S-parameters of GaN HEMT small signal model

Figure 7: Gain plots with two matching circuit design.

Fig. 8. The complete LNA design

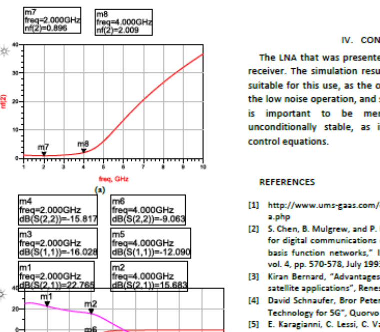

Fig. 9. a) Noise figure of figure 17 design, b) S-parameters of figure 17 design

IV. CONCLUSION

The LNA that was presented will be used in a wideband receiver. The simulation results show that its operation is suitable for this use, as the objectives were achieved: first the low noise operation, and second the high gain. Finally it is important to be mentioned that the LNA is unconditionally stable, as it results from the stability control equations.

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4. Παρουσιάσεις σε διεθνείς επιστημονικές συναντήσεις

1. Συμμετοχή στο 40th TCM CapTech Meeting, 17 Σεπτεμβρίου 2018, EDA, Βρυξέλλες, Παρουσίαση του ΡΑΝΤΑΡ

2. Ε. Καραγιάννη "State of the Art Ka-band MMICs using Stripline & Coplanar Techniques in Filters & GaN/Si High Power Amplifiers Design", Συμπόσιο Επιστήμης &Τεχνολογίας, ΛΑΕΔ, ΥΠΕΘΑ (ΓΔΑΕΕ-ΔΑΕΤΕ) Science & Technology Symposium, Oct. 22-23, 2018

ΕΛΛΗΝΙΚΗ ΔΗΜΟΚΡΑΤΙΑ
ΥΠΟΥΡΓΕΙΟ
ΟΙΚΟΝΟΜΙΑΣ & ΑΝΑΠΤΥΞΗΣ
ΕΙΔΙΚΗ ΓΡΑΜΜΑΤΕΙΑ ΕΤΠΑ & ΤΣ
ΕΙΔΙΚΗ ΥΠΗΡΕΣΙΑ ΔΙΑΧΕΙΡΙΣΗΣ ΕΠΑνΕΚ

ΕΣΠΑ 2014-2020
ανάπτυξη - εργασία - αλληλεγγύη

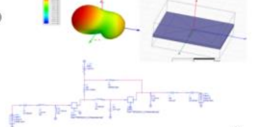
Με τη συγχρηματοδότηση της Ελλάδας και της Ευρωπαϊκής Ένωσης

RADAR

Electronics Laboratory - HNA
Combat Systems, Naval Operations, Sea Studies, Navigation, Electronics & Telecommunications Sector

Research Interests

- Monolithic Microwave Integrated Circuits (Design and Optimization)
- Microwave microstrip-stripline filters up to 40 GHz (ADS)
- Microwave Power Amplifiers and Microwave Low Noise Amplifiers in MIC and MMIC technologies (ADS)
- Microstrip Antennas (HFSS-CST)
  - Millimeter Wave Circuit Design
  - Ultra Wide Band Applications
  - Metamaterials



Collaborations

- Marine Materials Laboratory – Mechanics and Materials Sector – HNA
- Microelectronics Group – Institute of Electronic Structure and Laser - Foundation of Research and Technology – Hellas (MRG/FORTH)
- Microwaves and Fiber Optics Laboratory - Institute of Communication and Computer Systems - School of Electrical and Computer Engineering - National Technical University of Athens
- Electronics Laboratory – Department of Informatics and Telecommunications – National and Kapodistrian University of Athens
- Intracom Defense Electronics
- Prisma Electronics
- Institute of Nanoscience and Nanotechnology (INN) - Research Centre for Nuclear Research - Demokritos

Filters

- State of the Art Ka-band MMICs using Stripline Techniques in Filter Design

Stipline BandPassFilter Design

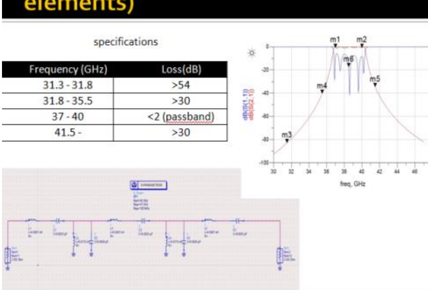
- Determining the type and order of approximation functions to be used.
- Finding the corresponding low-pass prototype.
- Transforming the low-pass network into a bandpass configuration.
- Transforming the lumped element into distributed elements.

- Elliptic bandpass filters show **lower loss and better selectivity** than Chebyshev filters that have an equal number of resonators. So, they are well suited for **microstrip applications**. However, because of the difficulty in realizing practical impedance levels, elliptic bandpass filters are not widely used in microstrip.
- Since Chebyshev filter has better roll-off than other filter types, this type of filter is chosen. The filter is designed by following the steps:

5th order Chebyshev BPF (lumped elements)

specifications

Frequency (GHz)	Loss(dB)
31.3 - 31.8	>54
31.8 - 35.5	>30
37 - 40	<2 (passband)
41.5 -	>30



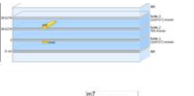
Ideal Coupled Transmission Lines

- Use equations for designing stripline BPF with N + 1 coupled line sections:
  - For 1st coupling $J_1 = \frac{1}{Z_0}\sqrt{\frac{\pi\Delta}{2g_1}}$
  - For intermediate coupling $J_n = \frac{1}{Z_0}\frac{\pi\Delta}{2\sqrt{g_n g_{n-1}}}$
  - For final coupling $J_{N+1} = \frac{1}{Z_0}\sqrt{\frac{\pi\Delta}{2g_N g_{N+1}}}$

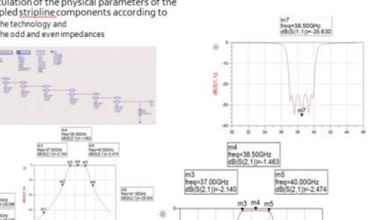
- Then, we obtain even and odd mode characteristic impedances

$$Zoe = Zo[1 + JZo + (JZo)^2]$$
$$Zoo = Zo[1 - JZo + (JZo)^2]$$

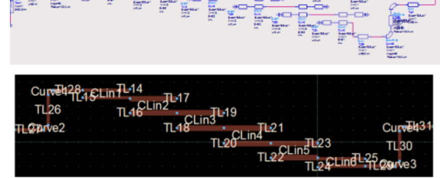
Stripline filter 5th Order (0.75mm)



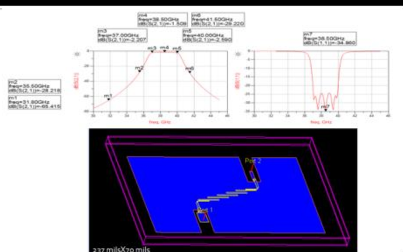
- Calculation of the physical parameters of the coupled stripline components according to
  - the technology and
  - the odd and even impedances



Design & Layout



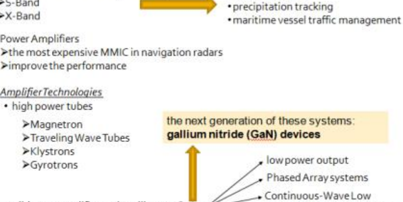
Stripline BandPass Filter



Amplifiers

- State of the Art Ka-band MMICs using Coplanar Techniques in GaN/Si High Power Amplifiers Design

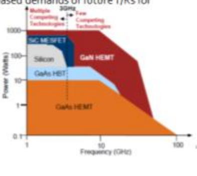
Power Amplifiers



Advances of GaN Technology

- The most common technology to replace GaAs is that of GaN due to a variety of superior material properties such as
  - High energy gap (3.4eV),
  - High critical electric field,
  - Higher load density and
  - High thermal conductivity.
- Support high power applications and hence a **smaller circuit area** for the same performance.
- A higher electron speed allows signal amplification at **higher frequencies**.
- GaN circuit devices can respond to the increased demands of future T/Rs for
  - greater power (over 40 dBm),
  - lower noise and higher operating frequency

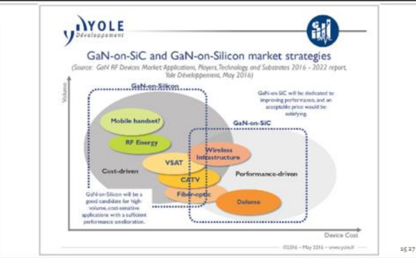
the system benefits
•at cost,
•at range and
•volume



GaN Technology

- GaN technology is a relatively new technology compared to other semiconductors, such as Si and GaAs, but the technology of choice for high frequency applications requiring higher energy and / or higher operating frequency is rapidly becoming available, such as **long distance signal transmission or at high power** (eg radar, base station transceiver - BTS, satellite communications, electronic interference - EMI and jamming, etc.).
- This technology, albeit new, already has dynamic entry into the markets. The adoption of GaN will ultimately lead to **lower costs** because:
  - (1) the complexity of the circuits is simplified
  - (2) the cost / watt is drastically reduced
  - (3) the operation time of the system is reduced because GaN devices require less energy and maintenance due to the durability of the material under adverse conditions (eg high temperatures).
- The new technology considered to be the successor of the circulator switches are the high-frequency microelectronic switches (**RF MEMS**) which at a typical operating frequency of 10GHz exceed
  - (a) input losses (0.1 dB instead of 0.8),
  - (b) M isolation (40dB instead of 17),
  - (c) have a smaller trace (0.9x0.9mm2 instead of 1.5x1.5mm2) and lower power consumption (RF MEMS switches have zero consumption).
- Lower-volume devices that operate at much higher power levels will encounter serious problems with increased levels of heat dissipation. The solution for future T/R (with better performance, less trace and volume and at a lower cost) is the combined use of GaN and RF MEMS supported by an **efficient platform for removing the heat produced**

GaN market strategies



Με τη συγχρηματοδότηση της Ελλάδας και της Ευρωπαϊκής Ένωσης

RADAR

Phased Array Radars

- excellent beam agility
- very reliable
- minimize radar cross section
- passive phased array: the only active elements are the phase shifters (extremely reliable)
- **Active Phased Array Radar Systems** have many advantages compared to passive
  - low loss
  - higher sensitivity
  - more reliable
  - increased capability

Passive

Active

16 27

GaN solid state amplifier design in the S-band 2.9-3.1 frequency region

- The TGF2023-01 is a discrete 1.25 mm GaN on SiC HEMT which operates from DC-18 GHz.
- Provides 38 dBm of saturated output power with power gain of 18 dB at 3 GHz.
- The maximum power added efficiency has a typical value of 55% and a maximum value of 66% which makes the TGF2023-01 appropriate for high efficiency applications.
- **Simulation target**
  - Gain>20dB
  - S11<10dB
  - S22<10dB
  - VSWR<3dB
  - Wideband Stability

0.25um GaN production process

Input matching circuit — Compromise between high gain and low noise figure

Intermediate matching circuit — Reduces the reflections between the two stages

Ensures maximum power transmittion

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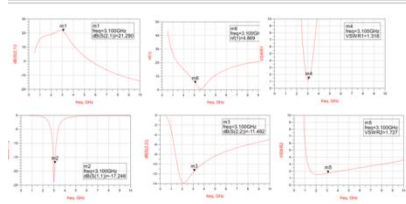
Simulation Results



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RADAR Project: "Heterogeneous Three-dimensional Integration using innovative nanotechnologies for the new generation of microwave power transceivers"

ΕΠΑνΕΚ 2014-2020 ΕΠΙΧΕΙΡΗΣΙΑΚΟ ΠΡΟΓΡΑΜΜΑ ΑΝΤΑΓΩΝΙΣΤΙΚΟΤΗΤΑ • ΕΠΙΧΕΙΡΗΜΑΤΙΚΟΤΗΤΑ • ΚΑΙΝΟΤΟΜΙΑ

- **EU, Action for Research, "Research - Creation - Innovation", 2014-2020, Operational Program "Competitiveness-Entrepreneurship-Innovation"**
- The project has three years duration (from now), seven institutions cooperate and the coordinator is the Foundation for Research and Technology (FORTH) of Crete.
  - Prisma Electronics
  - Global Nanotechnologies
  - Institute of Nanoscience and Nanotechnology "Demokritos"
  - National and Kapodistrian University of Athens
  - Hellenic Naval Academy
  - AMEN Technologies
- **The Hellenic Naval Academy as a partner has to design and optimize the GaN MMIC circuits: the High Power Amplifier (HPA) and the Low Noise Amplifier (LNA).**
- **Modeling will be done using electronic design and electromagnetic simulation software such as ADS, HFSS, EMPro and CST to achieve optimization of performance. The design library will be completed in parts through a sufficient number of feedback cycles to design, construct, characterize and compare between computational and experimental data.**

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HNA Projects

RADAR: "Heterogeneous Three-dimensional Integration using innovative nanotechnologies for the new generation of microwave power transceivers"

- Wireless and satellite communications, terrestrial and airborn radar, cable TV, intelligent transport infrastructure and the Internet of Things (IoT) are socially critical applications that have a significant impact on our everyday lives.
- All these applications are based on the use of transceivers (T/R) that allow the emission of electromagnetic (E/M) waves.
- The central element of the transceiver is the **RF front end** or Low Noise Block which is composed of -among others-
  - high power amplifiers (HPAs) for signal transmission,
  - low power amplifiers (LNAs) for reception of the signal,
  - a common transmit / receive antenna and
  - a switch that allows the transition from the transmitting circuit to the corresponding receive.

GaN/SiC substrate ~500μm

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T/R Re-designation: Demand

- The current industrial technology of the HPA "Output" Circuit (and "Input" LNA circuit) is based on GaAs semiconductor arrays that are hybridized to the antenna via a switching system (circulator switch) capable of electromagnetic (E / M) isolation.
- Upcoming applications such as 5G, IoT, autonomous vehicles, new generation active phase antenna radar have upgraded requirements such as
  - higher power,
  - higher operating frequency,
  - smallest footprint and volume,
  - enhanced functionality and
  - lower cost
- What is also worth mentioning is the attempt to exploit the terahertz gap that is now unlisenced, which will soon require reliable T/R.
- Consequently, transceivers need redesigning and introducing innovative solutions since GaAs and circulator switches are no longer capable of meeting the new requirements.

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RADAR Prototypes

- 1st Prototype (GaN/SiC)
  - X-band (8-12 GHz) operation with 50W output power. It will be demonstrated to a 8-element phased array system. Because of the high power, an innovative thermal platform will be developed based on Thermal Interface Materials-TIM as well as Thermo Electric Cooling - TEC, 3D integrated with the T/R.
- **2nd Prototype (GaN/Si)**
  - **Operate at Ka-band (26-40 GHz) with 30W output power and the corresponding thermal support**

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Hellenic Naval Academy Participation in RADAR

- **Leader WP 2.2: Design Library for the HPA & LNA**
  - For the performance optimization of the GaN MMIC circuits such as HPA, the modeling will be done using Electronic and Electromagnetic Software like ADS, HFSS, EMPro και CST. The design library will be completed in part through a sufficient number of feedback cycles to design, construct, characterize and compare computational and experimental data
- **Participation in**
  - **WP 2.4: Surface acoustic wave GaN sensor**
  - **WP 2.6: Si interposer** (Modeling and Optimization of the Through Silicon Vias –TSV structures that will serve as vertical vectors of the RF signal through the silicon interposer of the prototypes)
  - **WP 4.1: Prototypes Design** (RF, mechanical and thermal design for the metallic platform that will have the 4 or 8 T/R modules)

23 27

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  - **WP 4.1: Prototypes Design** (RF, mechanical and thermal design for the metallic platform that will have the 4 or 8 T/R modules)

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RADAR Prototypes

- The current state of commercial HPAs is that high output power (over 40W) is provided in zones L and C. In zone X the highest power value is 35W while in zone Ka the value is 15W. In general, commercial products are produced using the microstrip technique.
  - The first *HPA* will be produced with the coplanar technique with 50W power at X-band and 30W at Ka Band.
- The current commercial LNAs are up to 22GHz with noise figure (NF) 2.5dB.
  - Coplanar LNA with SotA performance will be produced. The emphasis will be on the Ka band targeting NF <1.7dB.

Properties	State-of-the-art		«RANDAR»	
	1st Prototype	2nd Prototype	1st Prototype	2nd Prototype
Frequency	No units	No units	X-band	Ka Band
Output Power (T)			50 W	35 W
Linear Gain (T)			21 dB	20 dB
Noise figure (R)			1.5 dB	<2 dB
Linear Gain (R)			25 dB	25 dB

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X-band (50W) T/R:

- The T/R of this category mainly targets the purchase of radar applications. According to a new Market Research Report "Purchasing Air Traffic Control Equipment" published by Markets and Markets (world leading market research firm), the global Traffic Control Equipment (ATC) market is expected to reach 5519.5M by 2020.
  - **This market demands relatively small number of T/R (~1000/radar) but the cost of every T/R may be reach 200-300€, so it is a *performance driven* application.**
  - The positive outcome will depend on:
    - (1) the transition of radar technology from today's brick technology to the predicted type of tile technology; and
    - (2) whether the new European safety standards RECAT-EU 2 and RECAT -EU3 requiring new technology, will be implemented based on the projected timeframe, ie 2020-21 in the 1st and 2022-23 in the 2nd.

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Ka-band (30W) T/R:

- T/R of this type is mainly aimed at cost-driven applications such as wireless communications (5G), satellite communications (SATCOM), stand-alone vehicles, satellite and cable TV and IoT. Purchases of RF GaN-based devices require a very large number of T/R (cost-driven).
  - A crucial factor in the commercial exploitation of these T/R will also be the time option to implement new standards in applications such as wireless communication (5G) expected for 2023 and the next generation SATCOM (2022).
  - Especially for 5G, an important factor will be the final choice of frequencies that with the international designs so far favors the choice of Ka band.
- "*Unique Business Window Opportunity" because* many and large companies produce power transceivers but there is none to supply monolithic integrated, parameterized - "smart" transceivers.

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Thank you for your attention

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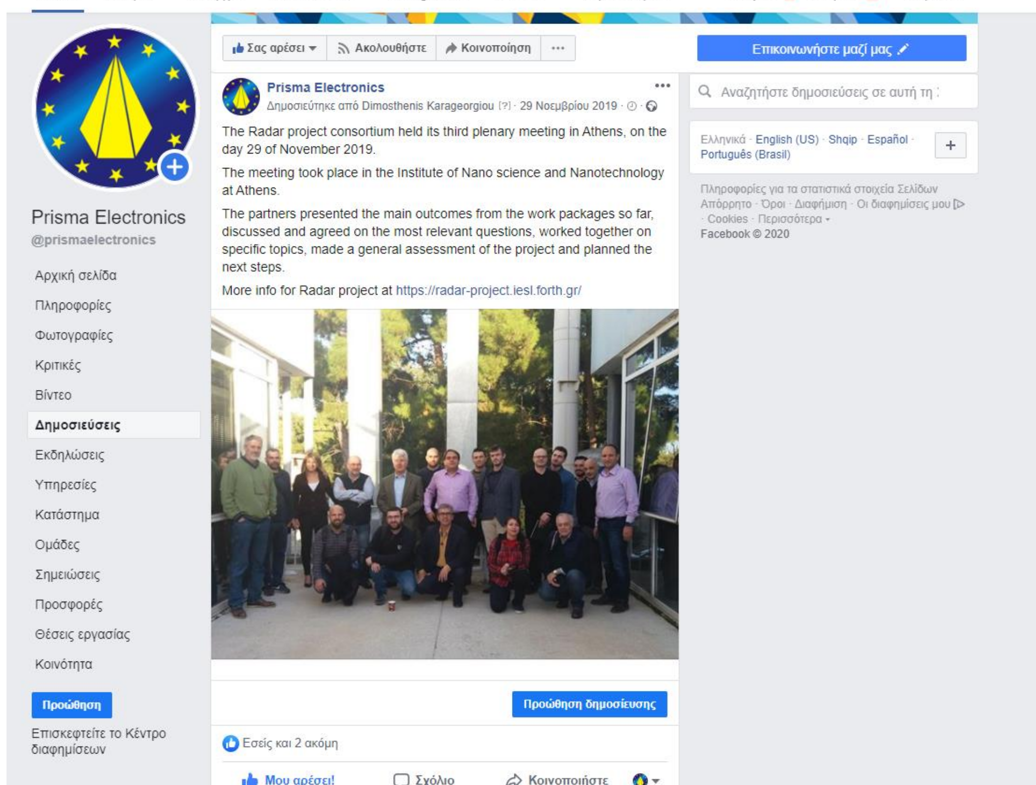
5. Προβολή σε Μέσα Κοινωνικής Δικτύωσης και Εταιρικές Ιστοσελίδες

1. Προβολή του έργου και της εξέλιξης του στα Μέσα Κοινωνικής Δικτύωσης.



https://www.prismaelectronics.eu/index.php/en/profil-en/news-en/186-the-radar-project-consortium-held-its-third-plenary-meeting-in-athens